**Amendments to the Specification:**

Please replace paragraph beginning at page 11, line 26, with the following amended paragraph:

Another insulating layer 30 (Figure 5E) formed from the photo-patternable low k dielectric material is deposited on liner 28. Layer 30 is exposed to light rays masked by mask 32 (Figure 5F) to define a trench and subsequently developed (Figure 5G) to form the trench. A liner 34 (Figure 5H) is deposited on the top surface of layer 30 and the sides of the trench to smooth these surfaces also. Copper conductor 20 is exposed by an etch of liner 34 (Figure 5I), a barrier layer of , for example, Ta, TaN, TiN, Ti(Si)N, or WN and a seed layer of copper (collectively 36) are deposited on liner 34 and the exposed surface ~~of insulating layers 16 and 30 and~~ of conductor 20 (Figure 5J), and copper 38 is electrodeposited in the via and the trench (Figure 5K). The copper is polished back to the surface of layer 30 (Figure 5L), and another copper barrier layer 40 (Figure 5M) is formed over the stack.

SILICON VALLEY
'ATENT GROUP LLP
50 Mission College Blvd
Suite 360
Santa Clara, CA 95054
(408) 982-8200
FAX (408) 982-8210